

Notice of References Cited	Application/Control No. 10/066,539	Applicant(s)/Patent Under Reexamination LIEN ET AL.	
	Examiner John J. Tabone, Jr.	Art Unit 2117	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
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	F	US-			
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Renovell, et al., Testing the configurable interconnect/logic interface of SRAM based FPGA's, IEEE, 9-12 March 1999 Page(s):618 – 622.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.